In the Claims

1. (Currently amended) ~~An~~ A fully differential interface circuit, comprising:

a digital signal processor (DSP) having a clock generator generating a clock signal having a voltage;

a data access arrangement (DAA) having a clock regeneration element; and

a charge pump, coupled between said DSP and said DAA, said charge pump providing operating power to said DAA, said charge pump doubling the voltage of said clock signal, and said clock regeneration element regenerating a clock signal that is essentially identical to the clock signal generated by said clock generator.

2. (Previously amended) An interface circuit as set forth in claim 1, wherein said charge pump comprises:

a first capacitive element having an input side connected to said DSP and an output side connected to said DAA;

a second capacitive element having an input and an output each connected to said DAA; and

a rectifying element coupled between the output side of said first capacitive element and said second capacitive element, said rectifying element receiving said clock signal from said DSP and doubling the voltage of said clock signal before passing said clock signal to said DAA.

3. (Original) An interface circuit as set forth in claim 2, wherein said DSP includes a clock generator generating first and second clock pulses out of phase with each

other by 180° and wherein said first capacitive element comprises:

a first capacitor coupled to receive said first clock pulse; and

a second capacitor coupled to receive said second clock pulse, wherein said first capacitive element continuously outputs a positive output voltage to said rectifying element.

4. (Original) An interface circuit as set forth in claim 3, wherein said rectifying element comprises a diode rectifier.

5. (Currently amended) An interface circuit as set forth in claim 4, wherein said ~~DAA includes a~~ clock regeneration element is connected in parallel with said rectifying circuit to remove DC level shift and regenerate ~~a~~ clock pulses for use by the DAA which ~~is~~ are essentially identical to the clock pulses output by said clock generator.

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6. (Original) An interface circuit as set forth in claim 5, wherein said second capacitive element comprises a storage capacitor which stores the charge transferred by said first and said second capacitors.

7. (Currently amended) A method of providing power to a data access arrangement (DAA) in an interface circuit of a telecommunication network when a telephone line connected to said interface circuit is in the on-hook state, said interface circuit including a digital signal processor (DSP) having a clock generator, said method comprising the steps of:

inserting a charge pump between said DSP and said DAA;

generating a power signal, having a voltage, across said charge pump by inputting the output of said clock generator to said charge pump; ~~and~~

doubling the voltage of said power signal and storing said generated power signal for use by said interface; and

regenerating a clock signal essentially identical to said output of said clock generator.

8. (Currently amended) ~~An~~ A fully differential interface circuit, comprising:

a driver circuit for developing a charge across capacitive elements of said interface circuit, said charge having a voltage, said driver circuit including a clock generator generating a clock signal;

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a data access arrangement (DAA) having a clock regeneration element; and

a charge pump, coupled between said DAA and said driver circuit, said charge pump providing operating power to said DAA, said charge pump doubling the voltage of said charge and passing said doubled voltage to said DAA to provide said operating power, and said clock regeneration element regenerating a clock signal that is essentially identical to the clock signal generated by said clock generator.

9. (Previously amended) An interface circuit as set forth in claim 8, wherein said charge pump comprises:

a first capacitive element having an input side connected to said driver circuit and an output side connected to said DAA;

a second capacitive element having an input and an output each connected to said

DAA; and

a rectifying element coupled between the output side of said first capacitive element and said second capacitive element, said rectifying element receiving said charge from said driver circuit and doubling the voltage of said charge before passing said charge to said DAA.

10. (Currently amended) An interface circuit as set forth in claim 9, wherein said ~~driver circuit comprises a~~ clock signal generated by said clock generator ~~generating~~ comprises first and second clock pulses out of phase with each other by 180° and wherein said first capacitive element comprises:

a first capacitor coupled to receive said first clock pulse; and

a second capacitor coupled to receive said second clock pulse, wherein said first capacitive element continuously outputs a positive output voltage to said rectifying element.

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11. (Original) An interface circuit as set forth in claim 10, wherein said rectifying element comprises a diode rectifier.

12. (Currently amended) An interface circuit as set forth in claim 11, wherein said ~~DAA includes a~~ clock regeneration element is connected in parallel with said rectifying circuit to remove DC level shift and regenerate ~~a~~ clock pulses for use by the DAA which ~~is~~ are essentially identical to the clock pulses output by said clock generator.

13. (Original) An interface circuit as set forth in claim 12, wherein said second

capacitive element comprises a storage capacitor which stores the charge transferred by said first and said second capacitors.

14. (Cancelled)

15. (Previously amended) An interface circuit as set forth in claim 2, wherein said first capacitive element has a capacitance sufficient to create said charge pump.

16. (Previously added) An interface circuit as set forth in claim 2, wherein the first capacitive element has a capacitance value of approximately 100 pF.

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17. (Cancelled)

18. (Previously amended) An interface circuit as set forth in claim 9, wherein said first capacitive element has a capacitance sufficient to create said charge pump.

19. (Previously added) An interface circuit as set forth in claim 9, wherein the first capacitive element has a capacitance value of approximately 100 pF.